Contents
Contents.............................................................................................................................. 1
Overview ................................................................................................................................ 2
What's New in Intel® IPP 2019 Update 3.................................................................................... 2
What's New in Intel® IPP 2019 Update 2.................................................................................... 3
What's New in Intel® IPP 2019 Update 1.................................................................................... 3
What's New in Intel® IPP 2019.................................................................................................. 3
Threading Notes....................................................................................................................... 4
Known Intel® IPP 2019 Update 3 Issues and Limitations.......................................................... 5
System Requirements ............................................................................................................. 5
Intel® IPP 2019 Documentation ............................................................................................... 5
Product Contents ................................................................................................................... 5
Intel® IPP Cryptography ........................................................................................................... 6
Technical Support .................................................................................................................. 6
License Definitions .................................................................................................................. 6
Third Party Licenses ............................................................................................................... 6
Legal Information ................................................................................................................... 7
Overview
This document provides a general summary of new features and important notes about the Intel® Integrated Performance Primitives (Intel® IPP) library software product.

Please see the following resources available online for the latest information regarding the Intel® Integrated Performance Primitives (Intel® IPP):

- Intel® IPP Main Product Page
- Intel® IPP Installation Guide
- Intel® IPP 2019 System Requirements
- Intel® IPP Documentation

Please register your product using your preferred email address. This helps Intel recognize you as a valued customer in the support forum and ensures that you will be notified of product updates. You can read the Intel Privacy Policy if you have any questions regarding the use of your email address for software product registration.

What's New in Intel® IPP 2019 Update 3

- Extended Intel® AVX2 and Intel® AVX-512 optimization for ippsFIRMR32f_32fc functions.

- Added a threading layer example on building custom pipeline code with the sobel filter functions.

- Added new implementation in the IIR Filter functions to improve precision. The implementation provides similar performance for long length vectors, but reduces the performance for short length vectors.

- Fixed several bugs in the bzip2 optimization patch files, including Makefile errors, and inconsistency with original code.

- Fixed the following dispatching issues in Intel® IPP libraries:
  - The IPP functions dispatched Intel® AVX2 optimization code on the Intel® AVX-512 processors with macOS* systems.
  - The cryptography libraries dispatched incorrect code on the systems that do not support Intel® AVX instructions.
  - The cryptography libraries dispatched incorrect optimization code when the libraries were linked dynamically.
What's New in Intel® IPP 2019 Update 2

- Intel® IPP Update 2 includes functional and security updates. Users should update to the latest version.

- The previous version of Intel IPP Custom Library Tool is removed in the releases. Users can use the new version of Intel IPP Custom Library Tool based on Python*.

What's New in Intel® IPP 2019 Update 1

- Added new functions to support SM2 public key cryptographic algorithm.

- Added support for Universal Windows driver and Universal Windows Platform (UWP) in the sequential static libraries.

- Added optimization for Intel® AVX-512 instruction set in the ippsFIRMR32f_32fc functions.

- Added support for Android* OS and Threading Layer libraries in the Intel IPP Custom Library Tool based on Python*.

- Removed support for IA-32 libraries on macOS* in this release.

What's New in Intel® IPP 2019

- Added new functions to support ZFP floating-point data compression and decompression. This release also introduces the optimization patch files for ZFP 0.5.2 source to provide drop-in optimization with the Intel® IPP functions.
  - ZFP is a lossy floating point data compression with controlled compression accuracy and compression rate. Intel® IPP ZFP functions are highly optimized for Intel® AVX2 and Intel® AVX-512 instruction sets.
  - Intel® IPP ZFP provides easy-to-use interfaces which allow for use of its functions directly in application source code. Intel® IPP ZFP also provides drop-in optimization patch files for open-source ZFP 0.5.2. Users’ applications can use open-source ZFP library interfaces with Intel® IPP optimized functions.

- Added Intel® Threading Building Blocks threading technology support in the Threading Layer APIs. Check the “Threading Notes” bellow to get more information.

- Added new version of Intel IPP Custom Library Tool based on Python*. This version provides better compatibility on different operation systems. The previous version of
Intel IPP Custom Library Tool is deprecated and will be removed in the future Intel IPP releases.

- Added new APIs to compute CRC24 and CRC16 checksum with 1U input data. The APIs support CRC24A, CRC24B, CRC24C and CRC16 polynomial functions, and are included in the Intel® IPP embedded domain.

- Color Conversion:
  - Added color conversion functions to convert RGB image to CIE Lab color model, or CIE Lab color model to RGB (ippiRGBToLab/ippiLabToRGB).

- Data Compression:
  - Added the optimization patch files for the bzip2 source to provide drop-in optimization with Intel® IPP functions. The patches now supports bzip2 version 1.0.6.

- Performance:
  - Extended optimization for the Intel® Advanced Vector Extensions 512 (Intel® AVX-512) instruction sets.

- Other Changes:
  - Removed support for Intel® Xeon Phi™ 72** product family coprocessor (formerly code name Knights Landing) on Windows* platform in this release.
  - Removed support for Intel® Quark™ microprocessors in this release.
  - The IA-32 libraries on macOS* are deprecated and will be removed in a future release.

**Threading Notes**

Intel® IPP provides Threading Layer APIs on top of sequential Intel® IPP libraries. The APIs include two variants 1) functions with _T suffix in the names, providing threading implementation based on classic IPP APIs; 2) functions with _LT suffix, providing threading implementation based on Intel IPP Platform-Aware functions. The Threading Layer APIs support both OpenMP* and Intel® Threading Building Blocks threading technology. Source code of Intel® IPP Threading Layer is also available in IPP package as example and basis to organize threading for pipeline inside a customer application.

The legacy Intel IPP threaded libraries are still available by custom installation, and the code written with these libraries will work as before. However, the threaded library will
not expand its threading functions, and the new threading will be developed only in the new Intel® IPP threading layer APIs.

User applications are recommended to use the new Intel® IPP Threading Layer APIs or implement the threading based on IPP Threading Layer source code examples in their applications. Check the “Threading Layer Functions” section in the Intel® IPP Developer Reference, to get more information on these APIs.

**Known Intel® IPP 2019 Update 3 Issues and Limitations**

- The Erode and Dilate APIs added additional optimization branches. Some optimization branches have performance degradation on the Intel® AVX optimization code.

- The threading layer examples on macOS* fail to build because of the incorrect Makefile. To work around the issue, remove `intel64/` suffix from `G_IPP_PATH_SUFIX` variable in the `components/interfaces/tl/Makefile_base.mk` file.

**System Requirements**

For information about the Intel® IPP system requirements, please visit the Intel® Integrated Performance Primitives (Intel® IPP) 2019 System Requirements page.

**Intel® IPP 2019 Documentation**

Starting with this version of Intel IPP, most of the documentation is only available online at Intel® Software Documentation Library. You can also download it from the Intel® Software Development Products Registration Center > Product List > Intel® Parallel Studio XE(or Intel® System Studio) Documentation.

**Product Contents**

The Intel® IPP for Windows*, Linux* OS, and macOS* is provided as part of the Intel® Parallel Studio XE and Intel® System Studio product. It is also available from the free Intel® performance libraries program:

- Installation package only supports 64-bit host system. It includes both the 64-bit and 32-bit target libraries.
- Installation package also provides the online installer that downloads materials chosen during installation

Intel® IPP Cryptography is provided as the following optional packages:

- Intel® IPP Cryptography for Windows*
Intel® IPP Cryptography

Intel® IPP Cryptography is a separate installation package that contains the binaries and header files needed to utilize the functions contained in the Intel IPP cryptography domain. To obtain the Intel IPP Cryptography libraries, please review the knowledge base article: where do I download the Intel® IPP cryptography libraries.

Intel® IPP Cryptography library is also available through open source. Visit the Intel® IPP cryptography open source page on GitHub to access the library source code.

Technical Support

If you did not register your Intel® software product during installation, please do so now at the Intel® Software Development Products Registration Center. Registration entitles you to free technical support, product updates and upgrades for the duration of the support term.


For general information about Intel technical support, product updates, user forums, FAQs, tips and tricks and other support questions, please visit http://www.intel.com/software/products/support/.

Note: If your distributor provides technical support for this product, please contact them rather than Intel.

License Definitions

Any software source code included with this product is furnished under a software license and may only be used or copied in accordance with the terms of that license. Please see the Intel® Software Products End User License Agreement for license definitions and restrictions on the library.

Third Party Licenses

Intel® Integrated Performance Primitives (Intel® IPP) includes content from several 3rd party sources that was originally governed by the licenses referenced below:

- zlib library:
zlib.h -- interface of the 'zlib' general purpose compression library version 1.2.8, April 28th, 2013

Copyright© 1995-2013 Jean-loup Gailly and Mark Adler
This software is provided 'as-is', without any express or implied warranty. In no event will the authors be held liable for any damages arising from the use of this software. Permission is granted to anyone to use this software for any purpose, including commercial applications, and to alter it and redistribute it freely, subject to the following restrictions

1. The origin of this software must not be misrepresented; you must not claim that you wrote the original software. If you use this software in a product, an acknowledgment in the product documentation would be appreciated but is not required.

2. Altered source versions must be plainly marked as such, and must not be misrepresented as being the original software.

3. This notice may not be removed or altered from any source distribution

Jean-loup Gailly Mark Adler
jloup@gzip.org madler@alumni.caltech.edu

• bzip2:
Copyright© 1996 - 2015 julian@bzip.org

Legal Information

By using this document, in addition to any agreements you have with Intel, you accept the terms set forth below. You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

A "Mission Critical Application" is any application in which failure of the Intel Product could result, directly or indirectly, in personal injury or death. SHOULD YOU PURCHASE OR USE INTEL'S PRODUCTS FOR ANY SUCH MISSION CRITICAL APPLICATION, YOU SHALL INDEMNIFY AND HOLD INTEL AND ITS SUBSIDIARIES, SUBCONTRACTORS AND AFFILIATES, AND THE DIRECTORS, OFFICERS, AND EMPLOYEES OF EACH, HARMLESS AGAINST ALL
CLAIMS COSTS, DAMAGES, AND EXPENSES AND REASONABLE ATTORNEYS' FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PRODUCT LIABILITY, PERSONAL INJURY, OR DEATH ARISING IN ANY WAY OUT OF SUCH MISSION CRITICAL APPLICATION, WHETHER OR NOT INTEL OR ITS SUBCONTRACTOR WAS NEGLIGENT IN THE DESIGN, MANUFACTURE, OR WARNING OF THE INTEL PRODUCT OR ANY OF ITS PARTS.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined". Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or go to:

BlueMoon, BunnyPeople, Celeron, Centrino, Cilk, Flexpipe, Intel, the Intel logo, the Intel Anti-Theft technology logo, Intel AppUp, the Intel AppUp logo, Intel Atom, Intel CoFluent, Intel Core, Intel Inside, the Intel Inside logo, Intel Insider, Intel NetMerge, Intel NetStructure, Intel SingleDriver, Intel SpeedStep, Intel Sponsors of Tomorrow, the Intel Sponsors of Tomorrow logo, Intel vPro, Intel Xeon Phi, Intel XScale, InTru, the InTru logo, the InTru Inside logo, InTru soundmark, Iris, Itanium, Look Inside, the Look Inside logo, MCS, MMX, Pentium, Puma, RealSense, skool, the skool logo, SMARTi, Sound Mark, Stay With It, the Engineering Stay With It logo, The Creators Project, The Journey Inside, Thunderbolt, the Thunderbolt logo, Ultrabook, VTune, Xeon, X-GOLD and XMM are trademarks of Intel Corporation in the U.S. and/or other countries.

*Other names and brands may be claimed as the property of others.

Microsoft, Windows, and the Windows logo are trademarks, or registered trademarks of Microsoft Corporation in the United States and/or other countries.
Java is a registered trademark of Oracle and/or its affiliates.

Copyright (C) 2011-2018, Intel Corporation. All rights reserved.
Intel’s compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice.

Notice revision #20110804